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Capacitors, Methods Of Forming Capacitors, and Methods Of Forming Capacitor Dielectric Layers

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Capacitors, Methods Of Forming Capacitors, and Methods Of Forming Capacitor Dielectric Layers

TECHNICAL FIELD

This invention relates capacitors, to methods of forming capacitors and to methods of forming capacitor dielectric layers.

BACKGROUND OF THE INVENTION

Capacitors are commonly-used electrical components in semiconductor circuitry, for example in DRAM circuitry. As integrated circuitry density increases, there is a continuing challenge to maintain sufficiently high storage capacitance despite decreasing capacitor area. A typical capacitor is comprised of two conductive electrodes separated by a non-conducting dielectric region. The dielectric region is preferably comprised of one or more materials preferably having a high dielectric constant and low leakage current characteristics. Example materials include silicon oxides, such as SiO_2, and Si_3N_4. Si_3N_4 is typically preferred due to its higher dielectric constant than SiO_2.

Numerous capacitor dielectric materials have been and are being developed in an effort to meet the increasing stringent requirements associated with the production of smaller and smaller capacitor devices used in higher density integrated circuitry. Most of these materials do, however, add increased process

complexity or cost over utilization of conventional SiO_2 and Si_3N_4 capacitor dielectric materials.

One dielectric region in use today includes a composite of silicon oxide and silicon nitride layers. Specifically, a first capacitor electrode is formed to have a silicon oxide comprising layer, typically silicon dioxide, of 6 to 10 Angstroms thereover. Such might be formed by deposition, or more typically by ambient or native oxide formation due to oxidation of the first electrode material (for example conductively doped polysilicon) when exposed to clean room ambient atmosphere. Thereafter, a silicon nitride layer is typically deposited by low pressure chemical vapor deposition. This can, however, undesirably produce very small pinholes in the silicon nitride layer, particularly with thin layers of less than 200 Angstroms, with the pinholes becoming particularly problematic in layers of less than or equal to about 75 Angstroms thick. These pinholes can undesirably reduce film density and result in undesired leakage current in operation.

One technique for filling such pinholes is to oxidize the substrate in a manner which fills such pinholes with silicon oxide material. For example, one such manner where the lower electrode material comprises silicon is to expose the substrate to suitable oxidizing conditions to cause silicon from the electrode and silicon from the silicon nitride to oxidize. Such forms silicon oxide material which thereby completely fills the pinholes and forms a silicon oxide layer typically from about 5 Angstroms to about 25 Angstroms thick over the silicon nitride. Wet oxidation conditions are typically used.

A second capacitor electrode is ultimately formed thereover, with the dielectric region in such example comprising an oxide-nitride-oxide composite. Typically achieved dielectric constant for such a capacitor dielectric region is about 5. Higher dielectric constant capacitor dielectric regions are of course desired, and it would be desirable to provide methods which enable utilization of silicon nitride and/or silicon oxide material dielectric regions if practical.

The invention was primarily motivated in improving dielectric constant of silicon nitride comprising capacitor dielectric layers having pinholes formed therein which are filled with silicon oxide material. However the invention is in no way so limited as will be appreciated by the artisan, with the invention only being limited by the accompanying claims as literally worded without narrowing reference to the specification, and in accordance with the doctrine of equivalents.

SUMMARY

The invention includes capacitors, methods of forming capacitors and methods of forming capacitor dielectric layers. In one implementation, a method of forming a capacitor includes forming first and second capacitor electrodes over a substrate. A capacitor dielectric region is formed intermediate the first and second capacitor electrodes, and includes forming a silicon nitride comprising layer over the first capacitor electrode. A silicon oxide comprising layer is formed over the silicon nitride comprising layer. The silicon oxide comprising layer is exposed to an activated nitrogen species generated from a nitrogen-containing plasma effective to introduce nitrogen into at least an outermost portion of the silicon oxide comprising layer. Silicon nitride is formed therefrom effective to increase a dielectric constant of the dielectric region from what it was prior to said exposing.

In one implementation, a method of forming a capacitor dielectric layer includes forming a silicon nitride comprising layer over a substrate. An outer silicon oxide comprising layer is formed over the silicon nitride comprising layer. The substrate is provided with the silicon nitride and the silicon oxide comprising layers within a plasma deposition chamber. The chamber includes a substrate receiver and a powerable electrode spaced therefrom, and the substrate is received by the receiver. A spacing between the receiver and the electrode of at least 0.1 inch is provided, with the substrate being received on the receiver. With such spacing, a nitrogen comprising gas is injected to within the chamber and with the electrode generating a plasma therefrom effective to

form an activated nitrogen species which diffuses into the outer silicon oxide comprising layer. Silicon nitride is formed therefrom in only an outermost portion of the silicon oxide comprising layer.

In one implementation, a capacitor includes first and second capacitor electrodes. A capacitor dielectric region is received intermediate the first and second capacitor electrodes. The capacitor dielectric region includes a silicon nitride comprising layer having an outermost surface which contacts the second capacitor electrode. The outermost surface consists essentially of silicon nitride. The silicon nitride comprising layer has a plurality of pinholes therein which are at least partially filled with silicon oxide material which is spaced from the second electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment in process in accordance with an aspect of the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a view of the Fig. 2 wafer fragment at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is an alternate view of the Fig. 2 wafer fragment at a processing step subsequent to that shown by Fig. 2.

Fig. 5 is another alternate view of the Fig. 2 wafer fragment at a processing step subsequent to that shown by Fig. 2.

Fig. 6 is a diagrammatic view of a plasma deposition chamber usable in accordance with an aspect of the invention.

Fig. 7 is a view of the Fig. 3 wafer fragment at a processing step subsequent to that shown by Fig. 3.

Fig. 8 is a view of the Fig. 4 wafer fragment at a processing step subsequent to that shown by Fig. 4.

Fig. 9 is a view of the Fig. 5 wafer fragment at a processing step subsequent to that shown by Fig. 5.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

A wafer fragment in process in accordance with the method of forming a capacitor in accordance with an aspect of the invention is indicated generally with reference numeral 10. Such comprises a bulk monocrystalline silicon substrate 12. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. An insulative layer 14, for example doped or undoped silicon dioxide, or silicon nitride, is formed over bulk substrate 12.

A first capacitor electrode material 16 is formed over insulative layer 14. At this point, or preferably later in the process, electrode material 16 is ultimately patterned/provided into some desired first capacitor electrode shape. Exemplary materials for electrode 16 include silicon (for example polysilicon) metals, conductive metal oxides, and any other conductive layer or layers. An exemplary thickness in one preferred embodiment, and particularly where

layer 16 comprises polysilicon, is 600 Angstroms. A first or inner silicon oxide comprising layer 18 is formed over, and "on" as shown, first capacitor electrode 16. An exemplary method for forming layer 18 is by oxidizing an outer portion of electrode material 16, for example by exposure to clean room ambient. This oxide layer is not preferred, but rather an effect of an exposed silicon or other oxidizable substrate. Typical thickness for layer 18 is less than or equal to 15 Angstroms. Layer 18 preferably consists essentially of silicon dioxide.

A silicon nitride comprising layer 20 is formed over first capacitor electrode 16 and in the illustrated preferred embodiment is formed on first or inner silicon oxide comprising layer 18. An exemplary thickness is from 30 Angstroms to 80 Angstroms. In but one embodiment, silicon nitride comprising layer 20 is formed to have a plurality of pinholes 22 formed therein. Such are shown in exaggerated width in the figures for clarity. In the illustrated embodiment, at least some pinholes extend completely through layer 20 to silicon oxide comprising layer 18. Silicon nitride comprising layer 20 might be deposited by any existing or yet-to-be developed technique, with chemical vapor deposition or plasma enhanced chemical vapor deposition being but examples. One exemplary process whereby a silicon nitride layer 20 is deposited by chemical vapor deposition includes NH_3 at 300 sccm, dichlorosilane at 100 sccm, 750 mTorr, 600°C, and 60 minutes of processing.

Referring to Fig. 2, a second or outer silicon oxide comprising layer 24 is formed over silicon nitride comprising layer 20, and as shown in the preferred

embodiment is formed thereon. In one preferred embodiment, and where silicon nitride comprising layer 20 includes pinholes, silicon oxide comprising layer 24 is formed effective to fill such pinholes with silicon oxide, as shown. Such preferably occurs by an oxidation. One example method of forming silicon oxide comprising layer 24 is to oxidize the substrate effective to both fill said pinholes with silicon oxide derived from at least some silicon of the first capacitor electrode material and form such second silicon oxide comprising layer 24 on silicon nitride comprising layer 20 thereover from at least some silicon of the silicon nitride material. By way of example only, exemplary oxidation conditions include 800°C, 5 slpm H_2, 10 slpm O_2, at atmospheric pressure for 15 minutes. For purposes of the continuing discussion, second silicon oxide comprising layer 24 upon formation includes a portion 25 which is everywhere received elevationally over silicon nitride comprising layer 20, and which is outside of pinholes 22. An exemplary thickness for portion 25 is from 5 Angstroms to 25 Angstroms.

The silicon oxide comprising layer is exposed to an activated nitrogen species generated from a nitrogen-containing plasma effective to introduce nitrogen into at least an outermost portion of the silicon oxide comprising layer, and silicon nitride is formed therefrom. By way of example only, Fig. 3, 4 and 5 illustrate different exemplary embodiments of the same where the silicon nitride comprising layer includes pinholes formed therein. Fig. 3 depicts wafer fragment embodiment 10, Fig. 4 an embodiment 10a, and Fig. 5 an embodiment 10b. Like numerals from the first described embodiments are

utilized in Figs. 4 and 5, with differences being indicated by different numerals or by "a" or "b" suffixes, respectively. In each of the depicted preferred embodiments, the exposing and forming of silicon nitride therefrom transforms only an outermost portion of the second silicon oxide comprising layer to silicon nitride. Alternately in accordance with an aspect of the invention, the entirety of a silicon oxide comprising layer received over a silicon nitride comprising layer might be transformed to silicon nitride.

Transformation of the respective illustrated portions of former silicon oxide comprising layer 24 ultimately to silicon nitride is depicted by the stippling intended to show the transformation to silicon nitride. For example, Fig. 3 depicts all of portion 25 of silicon oxide comprising layer 24 as being transformed to silicon nitride. Fig. 4 depicts an embodiment wherein only an outermost part of portion 25a is ultimately transformed to silicon nitride. The Fig. 4 embodiment shows approximately half of portion 25a being transformed to silicon nitride. Of course, more or less of portion 25 might alternately be transformed in connection with the Fig. 4 embodiment. In Fig. 5, the exposing and forming silicon nitride therefrom was also effective to transform an outermost portion 27 of the silicon oxide material within the pinholes to silicon nitride. Such depicts an approximate outermost portion constituting roughly one-third of the pinhole depth in Fig. 5, although more or less transformation of the subject silicon oxide material within the pinholes might be transformed in accordance with the Fig. 5 and similar embodiments. In each of the preferred Figs. 3-5 embodiments, at least some silicon oxide remains within the previously formed

pinholes, with the embodiments of Figs. 3 and 4 depicting processing whereby no silicon nitride is formed within pinholes 22.

Exemplary preferred processing by which such exposing and transformation to silicon nitride occurs is as described in U.S. Patent Application Serial No. 09/633,556 filed August 7, 2000, entitled "Transistor Structures, Methods of Incorporating Nitrogen Into Silicon-Oxide-Containing Layers, and Methods of Forming Transistors", listing Gurtej S. Sandhu, John T. Moore and Neil R. Rueger as inventors, and which is herein fully incorporated by reference. One preferred process for effecting the exposing and formation of silicon nitride is described with reference to Fig. 6. Such diagrammatically depicts a plasma deposition chamber 60. Such preferably constitutes a single wafer processor comprising a powerable electrode 62 and a wafer receiver or chuck 64. Receiver 64 might be heated or cooled from an appropriate power source. Receiver 64 and electrode 62 are received within chamber walls 66. By way of example only, an exemplary such reactor would be a high density plasma chamber from Applied Materials. Electrode 62 and receiver 64 are spaced from one another by a depicted distance 68. Typically and preferably, such spacing is adjustable by the operator. In one preferred embodiment, substrate 10 of Fig. 2 is provided within chamber 60 received by receiver 64.

Nitrogen is injected to within chamber 60, for example from one or more injection ports 70, and with electrode 62 a plasma 72 is generated therefrom effective to form the activated nitrogen species. In one most preferred embodiment, generated plasma 72 is spaced from the outer silicon oxide

comprising layer of substrate 10. Such is preferably accomplished by the control of spacing 68 and the powering of electrode 62 to, in the preferred embodiment, preclude plasma 72 from directly being exposed to the outer surface of substrate 10. One reason for preferably avoiding direct plasma exposure is to avoid possible plasma damage to underlying devices. The illustrated plasma 72 constitutes an exemplary remote plasma, wherein the actual plasma species is not provided directly in contact with substrate 10. Plasma generation outside of the chamber could also be utilized to generate the activated nitrogen. Preferred spacing 68 is at least 0.1 inch, more preferably at least 1.0 inch, still more preferably at least 2.0 inches, and even more preferably at least 4.0 inches. Exemplary preferred nitrogen gasses include one or more of N_2, NH_3 and NO_x. Other exemplary processing parameters are as described in U.S. Patent Application Serial No. 09/633,556 referred to above. In one preferred embodiment, the activated nitrogen species diffuses into the outer silicon oxide comprising layer 24, and silicon nitride is formed therefrom in only an outermost portion of the silicon oxide comprising layer.

Preferably, the electrode is powered at anywhere from 100 to 3000 watts, with an exemplary preferred pressure range during the processing being, for example, from 10 mTorr to 1 Torr. Chuck temperature is preferably maintained from, for example, room temperature to about 900°C. Preferred exposure times include from 5 seconds to 60 seconds.

The formation of silicon nitride therefrom might occur during such exemplary exposing. Alternately, such might occur afterward from conventional

subsequent wafer processing involving thermal exposure of the substrate, or by a dedicated thermal annealing step. For example and by way of example only, if wafer receiver 64 is maintained at a temperature of around 800°C or higher during the exposing, silicon nitride may inherently form during such exposing by the act of nitrogen diffusion into layer 24. Alternately by way of example only and if processing at lower temperatures, silicon nitride might subsequently be formed from the diffused nitrogen species by thermally annealing the substrate at a temperature of at least 600°C after the exposing for some suitable period of time to effect silicon nitride transformation.

Referring to Figs. 7, 8 and 9, a second capacitor electrode 40 is formed over the substrate. In the preferred and illustrated embodiment, second capacitor electrode material 40 is formed on (in contact with) transformed layer 24/24a/24b. An exemplary thickness range for layer 40 is from 300 Angstroms to 600 Angstroms. Second electrode material 40 might comprise the same or different materials from first electrode material 16. In the depicted and preferred embodiment, layers 18, 20 and transformed layer 24/24a/24b constitute a respective capacitor dielectric region which is received intermediate the first and second capacitor electrodes. Most preferably in accordance with the preferred embodiment, the exposing of silicon oxide comprising layer 24 and the transformation to silicon nitride is effective to increase a dielectric constant of the dielectric region from what it was prior to the exposing.

The invention also comprises capacitors independent of the method of fabrication. For example, Figs. 7, 8 and 9 depict capacitor dielectric regions

18/20/24, 18/20/24a and 18/20/24b. Each comprises a silicon nitride comprising layer 20/24, 20/24a and 20/24b, respectively, having outermost surfaces 45, 45a and 45b, respectively. Surfaces 45, 45a and 45b contact the respective second capacitor electrodes 40. Outermost surfaces 45/45a/45b consist essentially of silicon nitride. Silicon nitride comprising layers 20/24, 20/24a and 20/24b have a plurality of pinholes 22 therein which are at least partially filled with silicon oxide comprising material which is spaced from second electrode material 40. In the embodiments of Figs. 7 and 8, such provide examples wherein the pinholes are totally filled with silicon oxide material. The embodiment of Fig. 9 depicts but one example wherein the pinholes are only partially filled with silicon oxide material, and in such depicted and preferred embodiment where the pinholes comprise uppermost portions which are filled with silicon nitride material.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.